bus that operates at hundreds of megahertz. Figure 16.18 shows a hypothetical system architecture that employs source-synchronous interfaces. There are three ICs, and each IC is connected to the other two via separate interfaces. Each interface consists of two unidirectional buses. Unlike the receive clock, the transmit and core clock domains are merged, because this example does not require the core to operate at a different frequency from that of the bus. It would be easy to insert a FIFO, too, if a benefit would result from decoupling the bus and core frequencies. Clock distribution for this system is relatively easy, because each IC requires the same core clock frequency, but the interfaces are self-timed, which removes clock tree skew as a concern.

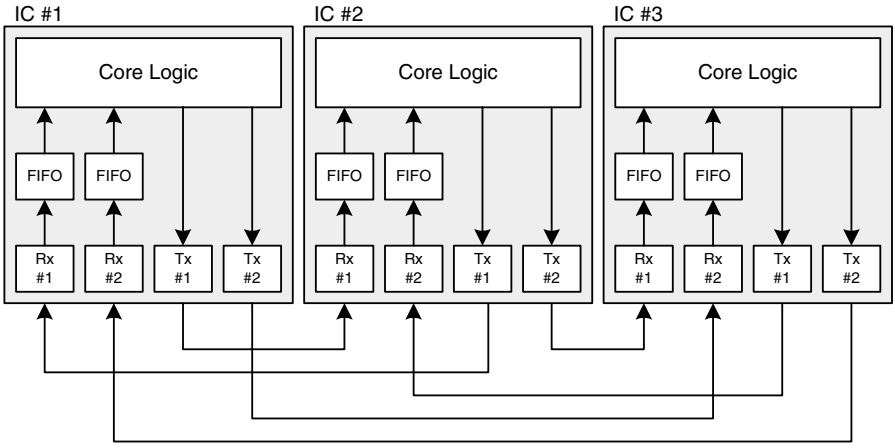

FIGURE 16.18 Source-synchronous system architecture.

CHAPTER 17
Voltage Regulation and Power Distribution

Power is an obviously critical component of a system, but some engineers have bad reputations for inadequately planning a system's voltage regulation and power distribution scheme. When power is an afterthought, luck sometimes works and sometimes does not. There is really no magic involved in designing an appropriate power subsystem, and this chapter seeks to explain the main issues that should be taken into consideration. The purpose of this chapter is to provide a broad understanding of power regulation concepts and how they can be applied to implement the power regulation and distribution circuitry in a digital system.

After many years of development and industry experience, we are fortunate to have at our disposal a broad array of off-the-shelf power regulation products. In concert with discrete semiconductors, a system's unique power requirements can be addressed with the appropriate tools. Many power requirements can be handled with off-the-shelf regulators. When situations arise that require a semicustom approach, the gaps can be filled in with a basic understanding of voltage regulation techniques.

Safety should be an overriding concern in all engineering disciplines, but safety is all the more critical when dealing with power circuits. Power circuits may carry potentially lethal voltages and currents and must be treated with a healthy respect. Resist the urge to quickly prototype a power circuit without taking the necessary time to study its thermal and electrical properties. Even if a power circuit appears to operate properly for a few minutes, an improper design can eventually overheat, with disastrous results.

This chapter is organized in two basic sections: voltage regulation and power distribution. First, basic voltage regulation principles are discussed to provide an orientation to the subject. Thermal analysis is then presented before any circuits are discussed, because thermal issues are fundamental to all power circuits. A safe and reliable circuit must be designed to handle its intended power load over its full range of operating conditions without overheating. The two subsequent sections deal with methods of regulating voltage and current, encompassing diode-shunt and transistor series-regulators. Off-the-shelf solutions are explored next to provide an understanding of the common integrated linear and switching regulators at an engineer's disposal.

Once basic regulation techniques have been presented, important issues in power distribution are discussed. Even the best regulator is useless without adequate means of conveying power to the load. Power distribution encompasses three basic themes: safety, reliability, and electrical integrity. Safety and reliability issues of handling AC power, fuses, and adequate wiring are discussed. Power regulation schemes employing precertified off-the-shelf AC-to-DC supplies are encouraged because of the improved safety of using known-good AC power modules. Finally, the use of low-inductance power planes and bypass capacitors is presented in the context of distributing power while preserving its electrical integrity. A brief power subsystem design example is used to illustrate these concepts.